22C:060: Computer Organization

Spring 2011

Assignment 5

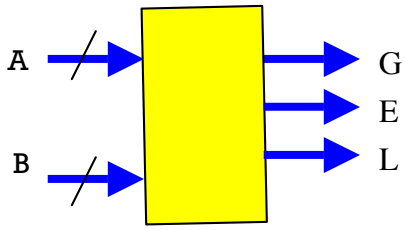
Total points = 50

Assigned April 14, due April 21, 2011, 11:59:59 PM

To submit, *zip* (or *tar*) all files into a single file, and drop it to ICON drop box

Question 1. (15 points) Show how to connect 4 (8K x 1 bit) RAM modules to design a (32K x 1 bit) memory. **A *clean diagram* with proper labels is essential**. Briefly explain how your design will work.

Question 2. (15 points)



Using a ROM chip (and nothing else), design a logic circuit to compare two 4-bit integers A and B, and produce three binary outputs: G (A greater than B), E (A equal to B) and L (A less than B). Thus if A = 14 and B = 8, then G=1, E=0, L=0, and if A = B = 12 then G=0. E=1, L=0.

(a) Explain your scheme, and show a part of the contents of the ROM locations. What will be size of the ROM?

(Hint: Somehow you have to enter the anticipated values of G, E, L into the ROM locations, so that the result is obtained by a simple table lookup. You can use (A, B) to address the ROM. Your answer need not show the contents of all the ROM locations, only 5-6 sample locations illustrating the design idea is sufficient.)

Question 3. (20 points) Consider a computer system with a single-level *direct-mapped cache* of size 128 bytes, and a main memory of size of 1 KB (i.e. 1024 bytes). Each line contains 8 bytes. A program running on this system accesses the following locations in consecutive steps:

10 1010 0100,
10 1010 1000,
10 1010 0100,
01 0000 0000,
00 1010 0000,
00 1010 1100,
00 1010 0100,
01 0000 0000,
10 1010 0000,
01 0000 0000.

Assuming that the initial contents of the cache lines are completely arbitrary, show which accesses will lead to a hit, and which will cause to a miss. Also, draw a table to show how the cache tags will change in each of the above steps.