# 22C:060: Computer Organization
# Spring 2010
## Assignment 6

Total points = 50

Assigned April 27 due May 4, 2010, 11:59:59 PM

**Question 1**. (20+10=30 points)

Fig. 4.17 in your textbook shows the datapath as well as the control signals of a single-cycle version of MIPS that supports the instructions lw, sw, a few R-type instructions, and beq.

*Part 1.* Assume that the processor executes a program that consists of only **load (lw)** and **store (sw)** operations. Simplify the datapath of Fig. 4.17 by removing the unnecessary units and redundant signals so that it supports only **lw** and **sw** instructions (and not the remaining instructions). Show only those control signals that are required in this design. Assume ALUop =00 that sets the output of ALU control to 0010, regardless of the values of instruction [5-0] (so that the ALU performs the **add** operation)

*Part 2.* Derive logical expressions for each of these control signals as a function of the opcode bits [Op5 – Op0] (same as instruction [31-26]). Explain your derivation. (Hint: Tables 4.12, 4.13, 4.22 may be useful)

**Question 2**. (20 points)

Consider the execution of the following program on a *pipelined* MIPS:

```
lw    r1, 100 (r2)
addi  r1, r1, 8
sw    r1, 200 (r6)
```

List the hazards posed by the pipelined datapath in the generation of the correct result. Assuming that a control unit resolves the hazards by inserting *bubbles* in the pipeline, *how many clock cycles* will be needed to complete the execution of the above three instructions? Use a timing chart to justify your answer.