22C:160/55:132 Homework 2 sample solutions

Chen Zhang

These are sample solutions, and there are other correct solutions too.
Question 1.
a) No additional components needed.

Fetch:	IR <= Memory[PC];
	PC <= PC + 4;
Decode:	A <= Reg[IR[25:21]];
Excution:	ALUOut <= A + sign-extend(IR[15-0])
R-Type Completion:	Reg[IR[15:11]] <= ALUOut

b) No addtional components needed.

Fetch:	IR <= Memory[PC];
	PC <= PC + 4;
Decode:	A <= Reg[IR[25:21]];
	B<= Reg[IR[20:16]] – assume these bits are all 0s
Excution:	ALUOut <= A + B
Completion:	PC <= ALUOut

c) A shift-left-16 component is needed for instruction[15-0] to multiplexer for ALU operand B.

Fetch:	IR <= Memory[PC];
	PC <= PC + 4;
Decode:	A <= Reg[IR[25:21]]; – assume these bits are all 0s
Excution:	ALUOut <= A + shift-left-16(IR[15-0])
Completion:	Reg[IR[20-16]] <= ALUOut;

Question 2.

Figure 1 shows the data path of such a processor.

Fetch:	IR < = IMemory[PC];
	PC <= PC + 6;
Decode:	A <= DMemory[IR[47-32]];
	B <= DMemory[IR[31-16]]
Excution:	ALUOut <= A - B
Completion:	DMemory[IR[31-16]] <= ALUOut
	if (ALUOut < 0) PC <= IR[15-0];

Figure 2 shows the state machine of this processor.

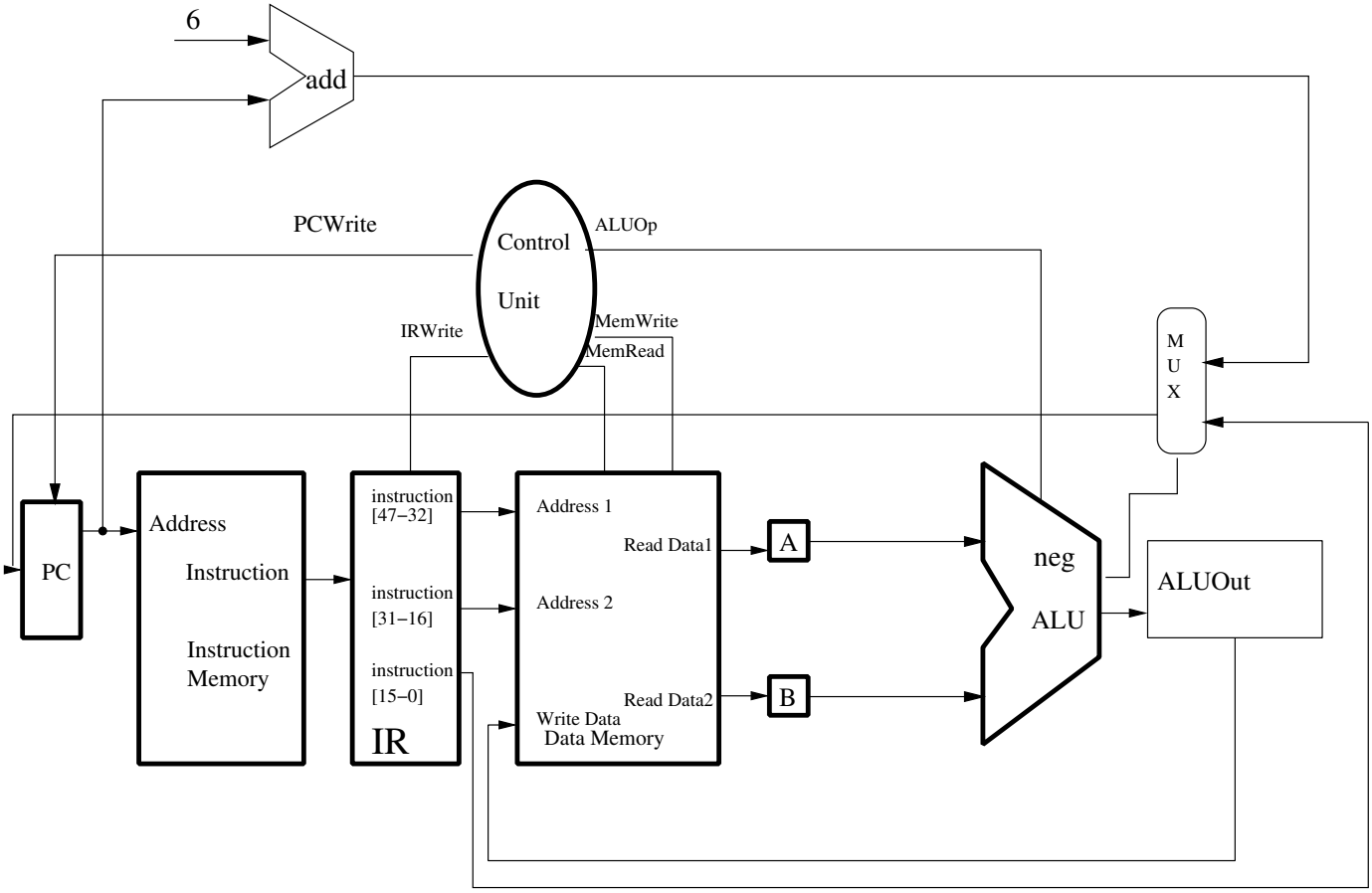

Figure 1: Datapath for 1-instrction processor

PCWrite = S0 +s3 MemRead = S1 MemWrite = S3 ALUOp = S2 IRWrite = S0

Question 3

add r3,r4,r2	F	D	X	M	W							
sub r5,r3,r1		O	O	F	D	X	M	W				
lw r6,200(r3)					F	D	X	M	W			
add r7,r3,r6						O	O	O	F	D	X	M	W

Achange in the order can save one cycle

add r3,r4,r2	F	D	X	M	W							
lw r6,200(r3)		O	O	F	D	X	M	W				
sub r5,r3,r1					F	D	X	M	W			
add r7,r3,r6						O	O	F	D	X	M	W

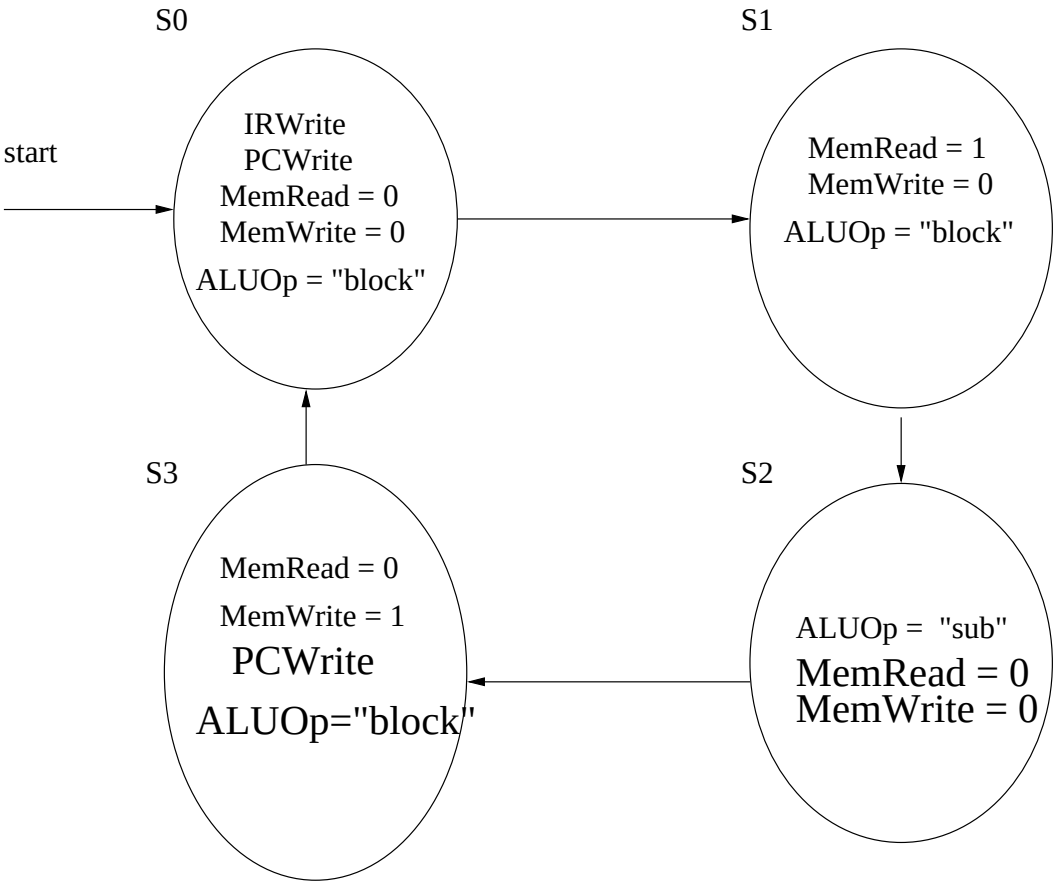

Figure 2: state machine